2023 Digital IC Design Homework 3

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| **Simulation Result** | | | | | |
| Functional simulation | | 100 | | Gate-level simulation | 100 |
|  | | | |  | |
| **Synthesis Result** | | | | | |
| Total logic elements | | | 465 | | |
| Total memory bits | | | 0 | | |
| Embedded multiplier 9-bit elements | | | 1 | | |
| Total cycle used | | | 2221 | | |
| Clock width | | | 40 ns | | |
| (your flow summary) | | | | | |
| **Description of your design** | | | | | |
| The proposed work is implemented using a finite state machine (FSM) that is divided into seven states. The state diagram is described below:    Given that interaction between the state is too complicated. We will give the brief description to the seven states.  IDLE: Resets all params and waits till the data inputs.  FETCH: Gets the input values and stores them into a predefined array.  PUSH: Pushes the input into the output array or operator stack.  POP: Pops the operator out to output array.  MERGE: Merges the operator stack and output array if the input all be scanned.  CAL: calculates the output array and returns the result.  FINISH: Rises the valid flag to outputs the result. | | | | | |

*Scoring = Area cost \* Timing cost*

*Area cost = Total logic elements + Total memory bits + 9\*Embedded multipliers 9-bit elements*

*Timing cost = Total cycle used \* Clock width*

**\* Total logic elements must not exceed 1500.**